Description of the Power Supply Control Scheme for the Spallation Neutron Source

BNL/SNS TECHNICAL NOTE

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PART I - FUNCTIONAL DESCRIPTION

SYSTEM FUNCTIONAL DESCRIPTION

Overview

Communications from a central control system to a power supply consists of three functions:

- Setpoint - This is an analog voltage representing the current to be regulated in the magnet load.
- Readback - Performance parameters are read back to the control system as analog voltages.
- Command/Status - Digital commands operate the supply, and status bits return state information.

System Configuration

These functions will be implemented with a single unit at the power converter, the Power Supply Interface (PSI), which will communicate with the control system through a Power Supply Controller (PSC). The identical interface will be used for all power supplies, and each power supply will have it's own PSI. Multiple PSI units (six to eight) will be controlled by a PSC.

A block diagram of the system configuration is shown in Figure 1.

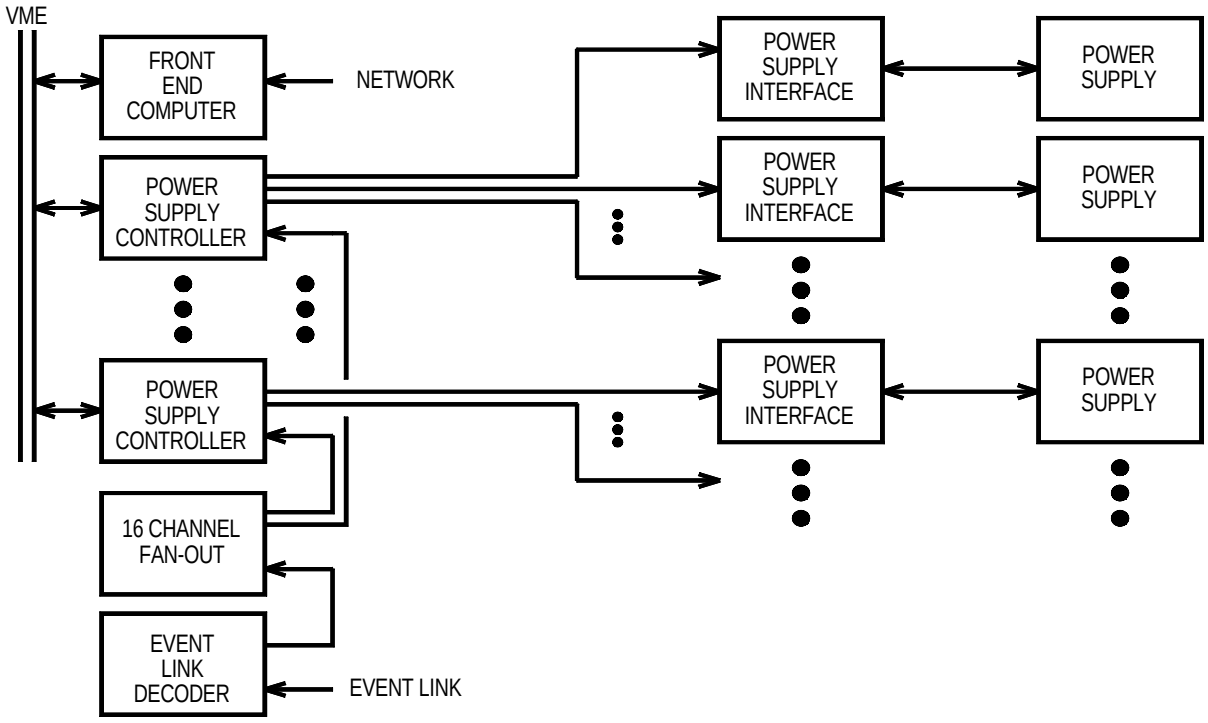


Figure 1. System Configuration

Each service building will have one or more control racks. These control racks will contain the front end computer and power supply controllers to service the power supplies in the entire building.

A single Power Supply Controller (PSC) will interface to multiple PSIs. It is now estimated that each PSC can handle six PSIs, but based on hardware design, that number may be as high as eight.

The connection between the PSC and the PSI is a pair of fibers - one to transmit data to the PSI, and the other to receive data from the PSI. The fiber pairs from each PSI go directly to a PSC. They are not multi-dropped to other PSI units.

This provides isolation between the control system and the power supply. And, as all control functions are provided by this single interface, no further isolation is required by the power supply or the control system. Each power supply has it's own PSI, and so each is isolated from every other by means of the control fibers.

Timing is provided by an event link decoder and fan-out modules to distribute the timing signals to the individual PSC units. There are two timing pulses, and they perform the identical operation with the exception that one pulse sends a setpoint command, and the other doesn't. A typical sequence is:

1. Data is sent from the PSC to the PSI.

2. The analog setpoint and digital commands in the PSI are updated (write pulse only).

3. The PSI reads the analog readbacks and digital status bits from the power supply.

4. Data is sent from the PSI to the PSC.

There will also be a burst mode, where a single pulse from the event timer initiates multiple sets of the typical sequence. This is described in greater detail in the Power Supply Controller section.

The Power Supply Controller

The Power Supply Controller ties together the major elements of the power supply control system:

1. It communicates with the front end computer (FEC), which sits in the same VME crate as the PSC. The FEC sends information, such as mode, and receives data back. There is also a RS232 interface on the PSC, that allows the PSC to be operated for test purposes.

2. It communicates with the event link decoder (through the fan out), which sets the timing of the data sequence.

3. It communicates with the PSI to send setpoint data and commands, and receives analog readback information and status bits. Sending data to the PSI is its timing signal. The data events in the PSI are timed by the PSC – one set of data from the PSI per transmission from the PSC.

The power supply controller block diagram is shown in Figure 2.

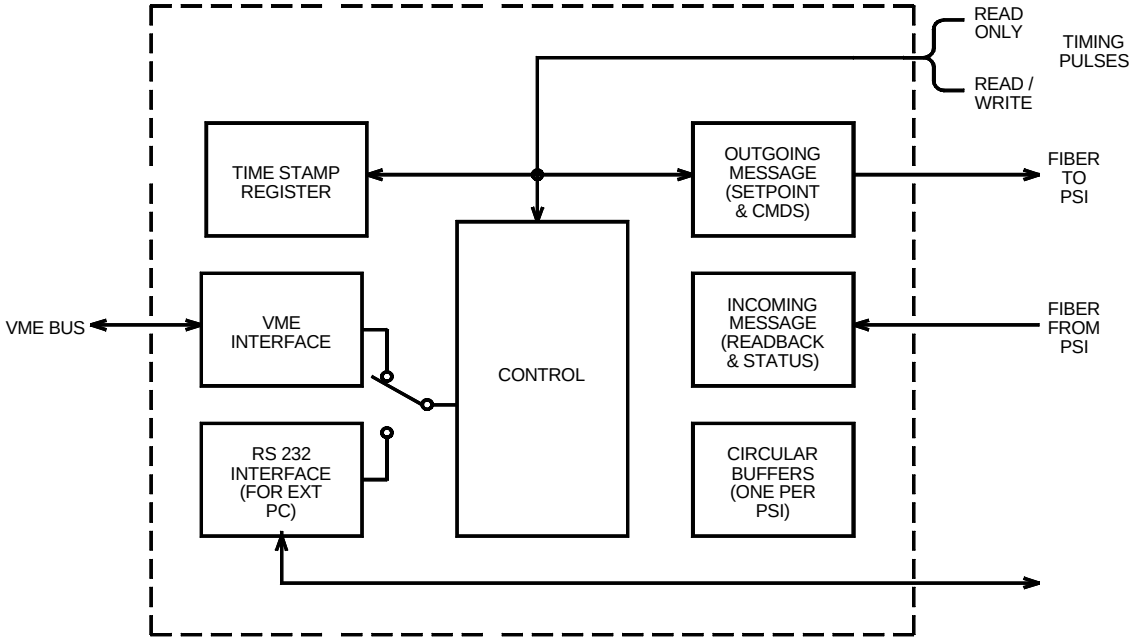


Figure 2. The Power Supply Controller

In addition to those sections already discussed, a time stamp register and a circular buffer can be seen. The time stamp buffer anchors the data to the machine cycle number, and the circular buffer provides a data history for each of the PSIs that the PSC controls.

There are two major modes of operation of the PSC. In the normal mode, each timing pulse from the event link initiates one data gathering cycle: sending data out to the PSI and getting data back into the PSC. This will typically be done at a 60Hz rate, and be synchronous with the beam.

A second mode, called the burst mode, is used to gather data with finer time resolution. Here, a single pulse from the event timer triggers a burst of data gathering cycles. The number and frequency of these cycles would be programmable by the FEC.

The burst mode can reveal synchronous information that happens at a rate faster than the 60 Hz beam rate. It can show the ripple of power supply. A twelve pulse converter, for example, would have a fundamental frequency of 720 Hz. It can also show the structure of the injection painting power supplies. This happens on a mSec time scale.

The Power Supply Interface

The block diagram of the PSI is shown in Figure 3.

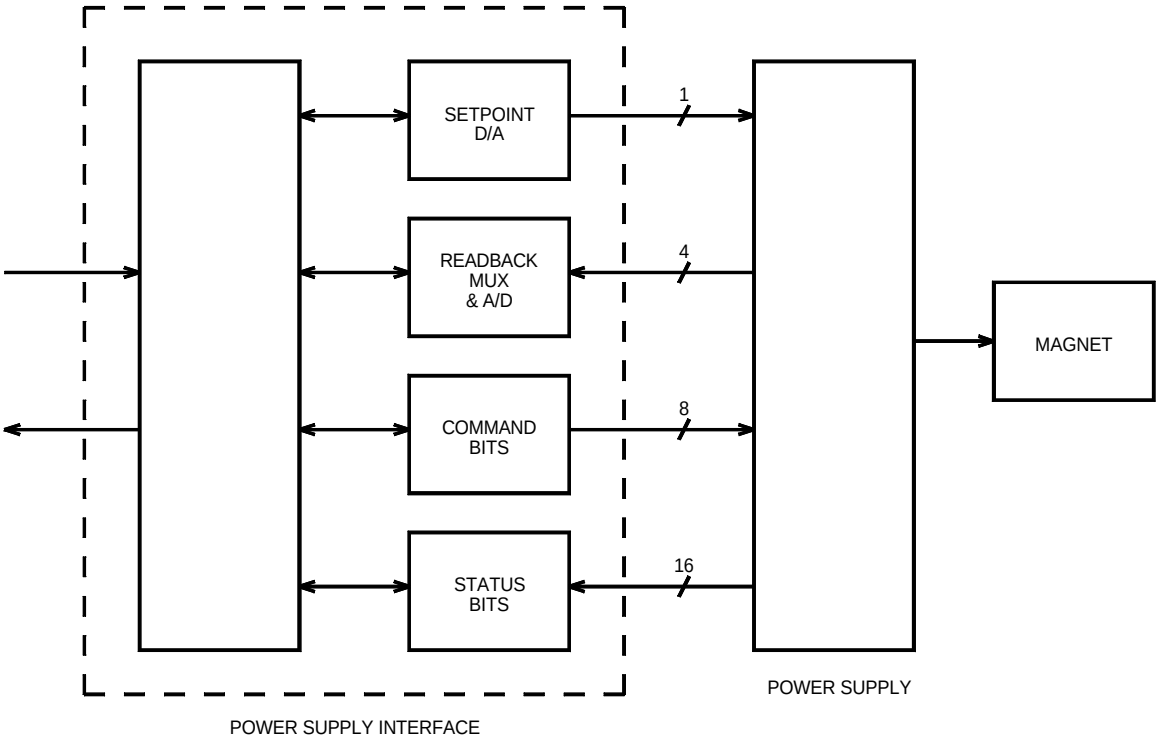


Figure 3. The Power Supply Interface

The major features of the Power Supply Interface are:

1. **Timing** - The PSC provides not only data, but also timing information. When the data arrives, it converts a new setpoint, and scans the readbacks. In doing so, timed setpoints and readbacks are implemented. In addition to power supply data, the PSI also returns information about itself. The data sent to the D/A is wrapped around digitally, and the configuration (polarity) is also returned.

2. **Setpoint** - The setpoint provides the analog interface to the power supply. The analog interface is based on a 16 bit resolution system with 15 bit stability to control supplies that have, at most, a stability requirement of one part in 10^4.

   The setpoint will be switch or jumper selectable to either unipolar or bipolar operation. The 16 bit number sent by the PSC will represent the full scale output current of the power supply being controlled. No scaling will be required by the PSI.

3. **Readback** - Four readbacks are provided to monitor power supply performance. Readbacks are always bipolar, regardless of how the setpoint has been selected.

    - Current Setpoint - The analog voltage from the PSI's D/A is converted back as a measure of both the D/A and the A/D. A voltage of 10V will represent full scale current.
    - Measured Current - A voltage representing the current as measured by a shunt or DCCT. A voltage of 10V will represent full scale current.
    - Measured Voltage - A voltage representing the power supply voltage. It includes both magnet and cable voltage drops. A voltage of 10V will represent full scale voltage.
    - Current Error - A voltage representing the current error, amplified within the power supply by a factor of 50. This helps see small regulation tracking errors, and may be of either polarity, even in a unipolar power supply. A voltage of 10V represents an error, which is 1/50 of the full scale current.

4. **Commands** - Eight command bits will be available. Many supplies may use as few as three of these. Others may use five. Currently, three bits are unallocated. All bits are TRUE high (15V), except for OFF, which is TRUE low (0V), to cause the power supply to shut off if the PSI loses power. All outputs are levels, but as the PSC communicates at a 60Hz rate, pulses can be programmed with that resolution.

    The allocated command bits are:

    - ON - Turns the power supply on.
    - OFF - Turns the power supply off.
    - STANDBY - Turns on control power in the supply, but does not energize the magnet load. In some supplies, this also resets faults.
    - RESET - Resets faults in supplies that require a separate line.
    - NEGATIVE POLARITY - Reverses polarity of current in the magnet to what is defined as negative.
    - Three unallocated command bits.

5. **Status** – Sixteen bits are available.

    - ON - Indicates that the power supply is on and delivering power to the magnet load.
    - OFF - Indicates that control power to the power supply is off, but AC power is available.
    - STANDBY - Indicates that control power to the power supply is on, but no power is being sent to the magnet load.
    - NEGATIVE - Indicates the power supply is in the reverse polarity.
    - FAULT SUMMARY - Indicates that a fault has shut down the power supply regardless of which fault it was.

- OVERVOLTAGE - Indicates that the power supply output voltage has exceeded it's set limit.
- OVERCURRENT - Indicates that the power supply output current has exceeded it's set limit.
- OUT OF REGULATION - Indicates that the current loop error is outside of acceptable limits.
- FAN FAULT - Indicates loss of air flow.
- OVERTEMP - Indicates excessive temperature anywhere in the power supply.
- WATER FLOW - Indicates loss of water flow.
- WATER MAT - Indicates water on the water mat, identifying a leak.
- SECURITY INTERLOCK - Indicates the power supply was shut down as a result of opening an external interlock contact.
- GROUND FAULT - Indicates a unwanted leakage path to ground.
- RIPPLE FAULT - Indicates excessive ripple, identifying a misfiring or failed SCR in a phase controlled power supply.
- PHASE FAULT - Indicates a lost phase or phase reversal.

MECHANICAL CONFIGURATIONS

PSI Standard Rack Packaging

The standard rack packaging of a PSI is shown in Figure 4.

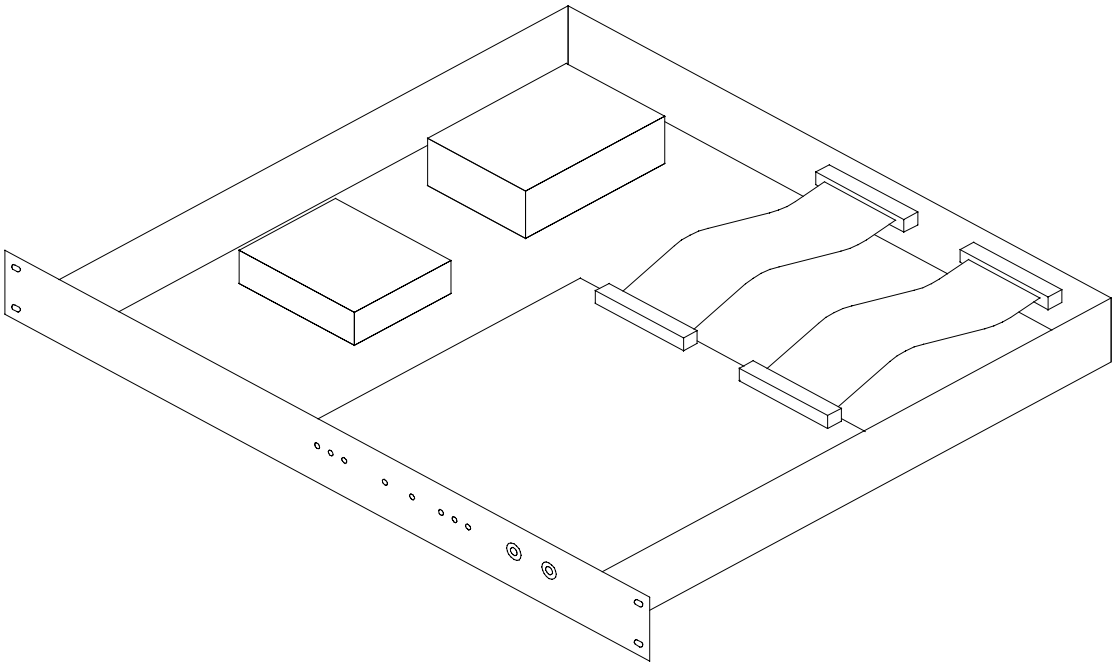


Figure 4. Standard Rack Packaging of PSI

This box contains the PSI itself, plus all power supplies needed for card. This makes it isolated from all other power supplies. The box is a standard width for a 19 inch equipment rack, and a height of 1U (1.75”).

This packaging configuration is suitable for small to very large independent power supplies.

PSI VME Packaging for Regulators

In those cases where there are large numbers of small power supplies, and those loads do not have to be electrically isolated, it is sometimes advantageous to have a single large AC to DC converter (bulk power supply), followed by a large number of regulators.

These small regulators can be packaged in a VME crate, and be low in cost. It is very advantageous for these units to have the same interface as the larger supplies, but the cost of these interfaces should be low also. We can accomplish this by designing the card in the standard rack packaging to be usable in a VME crate, by putting on a 4HP (0.8”) wide front panel. The result is shown in Figure 5.

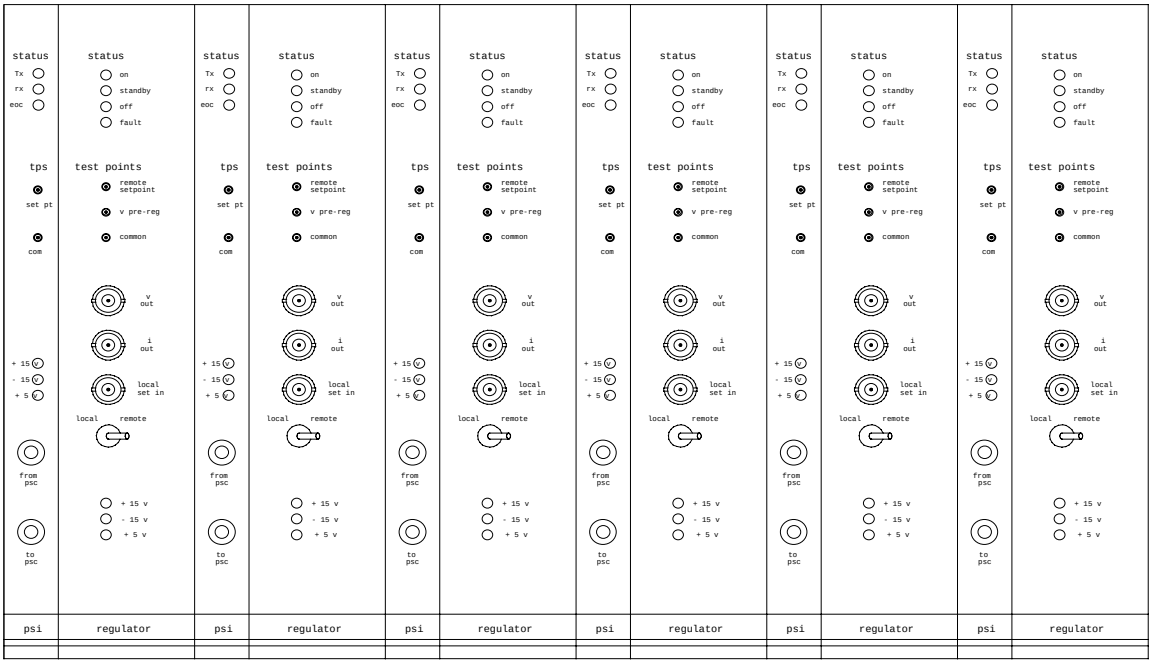


Figure 5. PSI and Low Current Regulators in a VME Crate

In each of the six pairs shown in Figure 5, there is a PSI in it's VME configuration, and a 10HP (2.0") wide regulator. When all six are mounted, they will fill up the standard 84HP width available in a VME crate.

The unit cost of the PSI in this configuration is lower because there are no individual power supplies and packaging for the card as there is with the rack mounted configurations. They will use a common set of power supplies, so there will not be any electrical isolation between these regulators. But, that is not a problem, as they share a common bulk supply, which makes isolation unnecessary. In addition, VME packaging concept requires a crate. That is also not a problem, as the crate is already required for the mounting of the regulators.

PSC VME Packaging

The Power Supply Controller is always packaged in a VME form. It sits in a crate along with the front end computer, event decoder, fan-outs, and other PSCs. Normally, the PSC will get it's information from the VME bus. But. the front panel of the PSC will have a serial port connector to permit commands (setpoints, controls) to be sent to the PSC, as well as reading data back from the PSI (readbacks, status).

Taken one step further, if we power the PSC card independently, we don't need anything else to test a "stand-alone" power supply. This is the idea behind the powered mini-VME crate.

The PSC in a Powered Mini-VME Crate

The serial port on the Power Supply Controller allows it (with a little packaging) to become an effective testing device. This is shown in Figure 6.

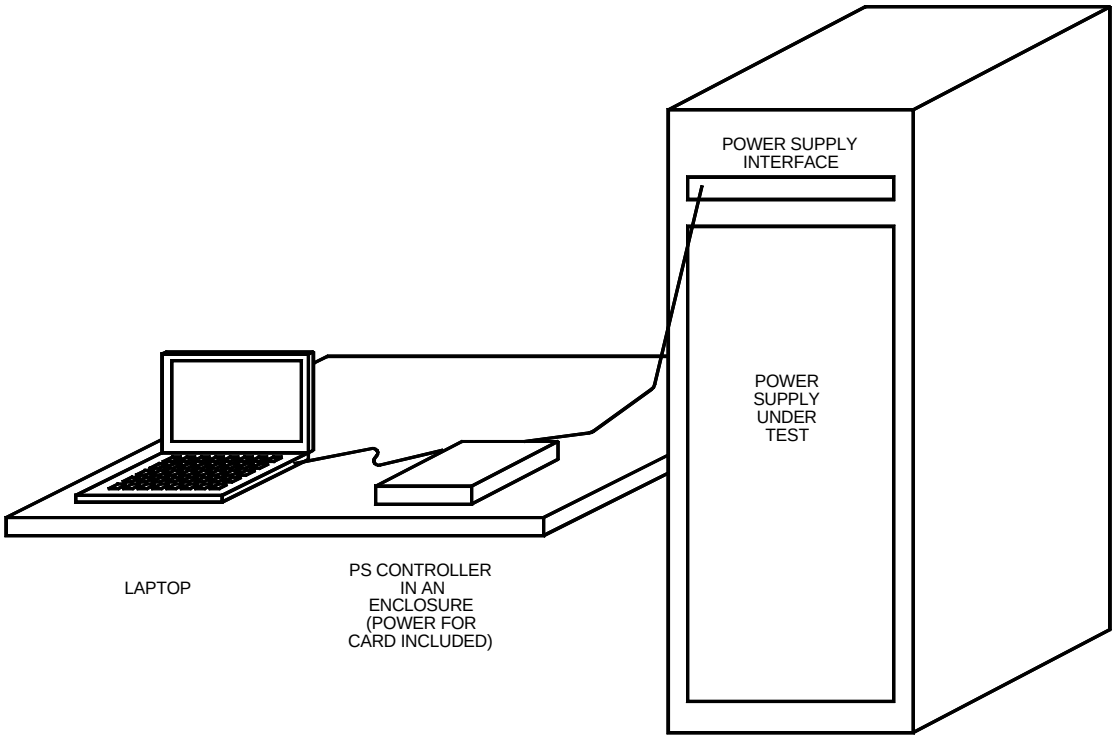


Figure 6. Testing the Control Interface

This permits software on the laptop to operate all the controls for the power supply. This is very useful for many reasons.

- The complete interface can be tested at the power supply manufacturer's facility. The unit can then be delivered directly to ORNL, and no further debugging will be needed.

- The power supplies can be tested with the magnet loads at ORNL, even if the control system is inaccessible for any reason.

- The test fixture can be used for off-line repair, when spare units have been used for replacements.

Aside from the PSC itself, few additional elements are needed. It will require:

- An enclosure to provide mounting and physical protection for the PCR, as well as supplies to power the card.

- An external timing source to simulate the event timer pulse. This would be plugged directly into the front panel connector on the PSC. If timing is not critical, the laptop can initiate messages over the RS-232 port.

- A personal computer. Software will be written to provide the functions necessary to control and gather data from the PSI.

ESSENTIAL FEATURES OF THIS INTERFACE SYSTEM

Simpler Interface for Power Supply Vendors

By simplifying the interface for the power supply vendors, we make the cost of those power supplies less, and maximize the number of vendors available to us. It gets us as close to an "off-the-shelf" unit as we can get.

The features that make this simpler for the power supply vendor are:

- **No isolation circuitry required** - The fibers and the PSI power supplies provide all the isolation that is required. That eliminates the need for the vendors to build in circuitry with both digital isolation and analog isolation.

- **No need to provide external power** – When packaged in the 1U chassis, the PSI has it's own power.

Self Contained Control System

Because the control system is integrated at the power supply vendor's facility,

- **There are no compatibility surprises** – The supply is integrated with the control system before the unit is shipped from the vendor. Even wiring mistakes should be eliminated.

- **On-site installation is nearly zero** – All that is required is to hook up two fibers. And, these can be prepared in advance.

Software Incompatibilities are Minimized

There are no concerns about updating PLC software to match changes in front end computer software.

Timed Readbacks

At first glance, it might seem odd to need timed readbacks for a DC machine. But, it is important for two reasons. First, you need to know what the current is *at the time the beam is present*. The average current may not be an accurate indicator of this due to:

- Outside disturbances – Line disturbances either due to the accelerator complex or not can be asynchronous, and their effect would not be detected in an average current monitor.

- Power supply malfunction – An increase in ripple is possible if a power supply starts to malfunction. A timed system can pick this up.

The second reason for timed readbacks is that, when combined with a circular buffer, they can provide failure data. Sometimes known as "glitch detection," this feature

captures the transient conditions just prior to and just after equipment shut-down. This can make locating and repairing problems much quicker.

Timed Setpoints

Timed setpoints are inherent in this system that has timed readbacks. Even in this very low bandwidth system of power supplies, that is an enhancement for two reasons:

- **Consistent and repeatable path** – While the system is nearly DC, changes will be made, and timed setpoints will create consistent and repeatable paths to those changes.

- **Interchangeability** – There are big advantages to SNS to have this system interchangeable with the largest group of accelerators. This is detailed further in the next section.

WIDER USE OF THIS CONTROL INTERFACE SYSTEM

Extending this Control System to Other Elements within SNS

While this control interface system was optimized for power supply control for the SNS project, this style of control can be extended to other accelerator elements on various levels.

- Standard power supply functions have been designed for the 8 bits of digital output and 16 bits of digital input for the PSI, but, these can carry any interpretation.

- It is important for isolation that a PSI controls only one device. But, there would be no problem in having two (or more) PSIs control one device. This would have application for two dimensional control.

- One can make other specialized interfaces, as was done here for power supplies. It may even be possible to use the same upstream devices (fiber, PSC, VME, …) as was done here, with those specialized interfaces. This should work well for elements which have large quantities of similar devices.

Extending this Control System to Other Accelerators

Developing a power supply interface system that will be usable for other accelerators is clearly useful for those projects, and in furthering the future DOE goals. Since it costs us essentially nothing to do this, that alone should be enough incentive to maintain this interface as general as possible.

But, the are also direct advantages to SNS:

- **Replacement units would be more easily available** – This is an advantage not only because it keeps these boards in production, but replacement units would be updated even if individual components become obsolete with time.

- **Upgrades can use designs from other projects** - It would make it easier to add features or experimental elements after construction is complete. Designs or even spare units can come from other projects

PART II - DETAILED DESCRIPTION

COMMUNICATION BETWEEN PSI AND PSC

Messages

A message from the PSI to the PSC consists of several frames. Each frame has a start bit, ID, Data, CRC and end bits. Messages from the PSC to the PSI will be one frame. The detailed format of the data transfers is given in the section, "DETAILED DESCRIPTION OF DATA FORMATS". A brief description follows here.

Messages sent from the PSC to the PSI

There are three types of messages that can be sent from the PSC to the PCI.

1. A write command that sends a setpoint.
2. A write command that sends command bits.
3. A read request.

Each message has an ID field which identifies the message type.

Messages sent from the PSI to the PSC

- Read Response

  The PSI sends a reply to the PSC after it receives a message from the PSC. In response to a read request the PSI returns eight frames. This same response will occur after a write request (either setpoint or command) if the “Read on Write” bit is set by the VME computer.

  1. An echo of the received data.
  2. Digital Setpoint (prior to the DAC)
  3. Digital Command
  4. Digital Status
  5. ADC 1 (Typically, analog setpoint)
  6. ADC 2 (Typically, analog measured current)
  7. ADC 3 (Typically, analog measured voltage)
  8. ADC 4 (Typically, analog measured voltage)

- Write Response

  In response to a write request where the “Read on Write” bit is not set, only one frame is returned – the echo of the received data.

Each frame contains a 16 bit word plus an 8-bit identifier. Each frame above has a unique ID value.

Message Timing

The data rate for frame transmissions will be 5 MHz. As each frame is 43 bits wide, it will require 8.6 microseconds for each frame to be transmitted.

The sequence of frames and the time budget for the complete exchange is as follows, for the longest case, which is the Status / ADC readback:

- One frame is sent from the PSC to the PSI: 8.6 µSec.
- The analog to digital conversion is initiated on receipt of the frame from the PSC. 20 µSec will be permitted for this conversion, after which the PSI will reply to the PSC: 20 µSec.
- A reply of six frames are sent from the PSI to the PSC: 8.6 x 6 = 51.6 µSec.

All together, the entire exchange will take 8.6 + 20 + 51.6 = 80.2 µSec. Considering the time to send the read request (10 µSec) and time to process the received data (5 µSec), the total time is 95.2 µSec, which allows a maximum repetition rate of over 10 KHz. We require a maximum read rate of 10 KHz in the burst mode.

POWER SUPPLY CONTROLLER (PSC)

Sending Messages

The power supply controller has two trigger inputs.

1. One will initiate a read command to the PCI board.
2. One will initiate a write command to the PCI board. Depending on the state set by the VME computer, this may be either a setpoint value or command bits.

We wish to have the capability to do timed settings. This is done by sending a message to the PSI on the occurrence of a write trigger. After setting the Setpoint or Command registers, the computer will set the Data Available Flag. When a hardware write trigger arrives, the Data Available flag is checked. If it is set, a write command is sent to the PSI with the data in the Setpoint/Command registers. Even if there is constant trigger input, a write command is only sent if the computer has set the data available flag.

The board does not require an external trigger. After writing new data to the Setpoint/Command register it can initiate a message by issuing the Set Data Available Flag and following it with a Send Command.

Trigger Overlap

It is assumed that one trigger (write or read) will not occur prior to the completion of the two way message of a prior trigger (approximately 95.2 µSec maximum, if the first pulse was a Read Status/ADC request). If this happens, the second trigger will not initiate a write or read, but if the second trigger was a read, it will increment the time counter.

Time Register

There will be a time count register on board the PSC. This register can be initialized over the VME bus. The register will be 16 bits. This register will be updated each time a read message is initiated, regardless if that be from the pulse input or the VME computer.

The time count register will not be updated when a write message is initiated, even if the write message causes a read reply.

Memory

All data coming to the computer will be stored in a local memory on board the PSC. There will be a 1 Megabit memory for each channel, with a minimum of six channels per board. On a Read Status/ADC request, 6 frames will be returned.

The first frame returned will be an echo of the data sent. When this frame is received the CRC value is checked and if an error is found, a error bit is set. For each frame received 4 bytes of data will be stored. For the second and subsequent frames the message id (8 bits), error bits (8 bits) and the upper 16-bits of the 24-bit data field will be stored.

When the first frame is received, the message id and the time register will be saved. Four bytes are saved for every frame received for a total of 32 bytes on each read request per channel.

We allow 8 error bits so that all data can be handled as 16 bit values. One error bit is reserved for CRC error. As described above, assuming the memory size is 128k bytes, and the read rate is 60 Hz, the memory can hold about 66 seconds of data.

There will be four modes of operating the memory. The mode commands will be initiated from the VME computer. When it is issued, the buffer is cleared. This can be done by setting the memory start address to 0.

1. ***Continuous*** mode - The memory is effectively a circular buffer. There is a counter to indicate the last address written.
2. ***Stop*** mode - This is used when you wish to read the buffer.
3. ***Stop on Full*** mode - In this mode the buffer is written until it is filled. This is transient mode recording. Data starts when transient mode is enabled and stops when transient mode is completed.
4. ***Stop at End of Burst*** mode – This mode is used to preserve the burst data.

Transmission Errors

When a frame is received the CRC is checked. If an error is found, an error bit is set, but an interrupt shall not be generated. When the computer checks for the data that was just read, it can monitor the error bit and take appropriate action. One action to be taken is the clearing of the error bit. Once the error bit is set, it stays set until cleared by the program. The error bit will be stored with the data. We will be able to define up to 8 error conditions per channel.

There will be a loss of carrier detector. A flag will be set for each channel indicating the carrier status. This will not be a bit in the data word since there will be no data if the carrier is lost. It will be a register that can be read by the computer.

Burst Mode

There will be a Burst mode to read data at a rapid rate. In this mode when a read pulse arrives, the controller will go into a burst mode. Instead of sending one read request, it will send N requests at an interval set by the computer. All channels will be in burst mode at the same time.

Two registers are required for this mode. One will let the computer set the number of messages. The second will let the computer set the rate. The number of messages will be between 100 and 4000 messages. The memory buffer size is approximately 4000 so there is no need to exceed this number. The rate will be between 500 and 10,000 Hz..

In burst mode, writing is disabled, as it will not be possible to have a write trigger and guarantee it will not overlap a write request.

In burst mode data is written to memory. The time flag is not updated on each read. It is only updated on the read request. This means that the time counter will be the same for several messages in the buffer. This is an indication of burst mode. The number of messages in the buffer with the same count is an indication of the rate.

RS-232 Input

Under normal conditions, communications to the PSC will be through the VME interface. However, as described earlier in this document, for testing situations, communication to the PSC will be through the RS-232 interface in the PSC itself.

The connection to this interface will be by a standard nine pin D connector, located on the front panel of the PSC.

All of the timing, command and data gathering capability of the VME interface, will be available to a computer attached to the RS-232 port.

VME INTERFACE

Messages Sent By A Command Via The VME Bus

Sending Data and/or Commands.

The VME computer has the following commands:

1. Prepare for Messages
   a) Write a new Setpoint to the Setpoint Register
   b) Write a new Command to the Command Register
   c) Set Read on Write bit – When set, the response to a write command will be a read reply. Otherwise, the reply from the PSI will only be an echo.
   d) Set Data Available Flag
   e) Set Burst Mode - This includes mode enable/disable, rate, and number of data points.

2. Initiate Messages
   a) Issue a Read Command
   b) Issue a Send Command

3. Set PSC States
   a) Set Time Counter
   b) Set Memory Mode – Continuous, Stop, Stop on Full, or Stop at End of Burst
   c) Set Unused Channels - Not every channel of the PSC will necessarily have a PSI connected to it. A command byte will be sent to the board to enable the active channels. Inactive channels will not cause a "loss-of-carrier" error bit to be set.

4. Memory Reads
   a) Read Data for Channel X
   b) Read Data from Memory for Channel X
   c) Read Memory Pointer
   d) Read Memory Mode

5. Status Reads
   a) Read Loss of Carrier bits - Flags set to indicate carrier status
   b) Read Trigger Overlap Error

Timing from the VME Bus

When the VME computer issues a Read or Write Command, the action to be taken by the PSC will be identical to the action taken when a hardware trigger is received.

VME Data Access

VME Reading Modes

There are two possible methods of reading data via the VME bus.

In the first case, the VME will have registers that can be accessed to acquire the last set of data received by the card. The system shall support D32, D16, and D08 addressing modes. Assuming 16-bit transfers, there will be sixteen 16-bit registers for each channel. For 32 bit transfers, there will be eight 32-bit registers. With this approach it is assumed that the VME computer will have to read the board at a time when the memory is not being updated. The VME computer would have to time its readings so as not to access memory when it is being updated. This implies that the VME would have to get an interrupt signal a fixed time before or sometime after the board received a trigger to read the data.

In the second case the VME will give a command to the PSC indicating that it wants to get the last reading for a particular channel. The board then transfers the data to VME accessible registers and sets a data available flag. Then the VME reads the data. In this mode, only 16 16-bit registers are needed. There is an advantage to this approach if it allowed access to PSC data without timed reads.

VME Read Access

It's expected that up to 12 of these boards will reside in one VME crate. There have to be board jumpers to set the starting address. The board will use 32-bit address space.

We expect that between 500 KBytes and 1 MBytes of data can be stored on board. For 12 boards this makes 6 to 12 MBytes of data that must be retrieved. We wish to be able to access this data in the lowest amount of time. Board access time should be less than 0.5 microseconds for a 4 Byte transfer. To reduce the read time we request 32 bit transfers. The board should be designed so the access time is a minimum.

POWER SUPPLY INTERFACE (PSI)

Analog Interface

Analog to Digital (ADC) Conversion

The PSI is required to convert four analog voltages to digital numbers for transmission back to the PSC. It will have four separate ADCs rather than one ADC and multiplexing switch. Doing so allows the ADC to have a 20 µSec conversion time, which permits a burst mode of up to 10 KHz, while being commercially available at an economical cost. Further, having four separate ADCs eliminates the switching transients that are inherent in multiplexing switches.

The timing of the start of conversion is important. It must occur only in response to a read request from the PSC.

Each ADC converter will have the following features:

- Resolution - 16 bits
- Accuracy - 15 bits
- Conversion time - 20 µSec
- Analog input - Bipolar ± 10 Volts

Digital to Analog (DAC) Conversion

The PSI is required to convert one digital number from the PSC to an analog voltage. The DAC will have the following features:

- Resolution - 16 bits
- Accuracy - 15 bits
- Conversion time - 20 µSec
- Analog output - Bipolar ± 10 Volts

Digital Interface

Digital Outputs

The PSC provides digital outputs to control the power supplies. The digital outputs will have the features:

- Levels - 15 Volt CMOS levels
- Drive capability - Sink or source at least 1 mA.

Digital Inputs

The PSI provides digital outputs to control the power supplies. The digital outputs will have the features:

- Levels - 15 Volt CMOS levels
- Drive requirements - Sink or source no more than 1 mA.

DETAILED DESCRIPTION OF DATA FORMATS

Communication Format

Communication between the PSC and the PSI is via 62 micron multimode fiber. Two fibers, one receive and one transmit, will be used between the PSC and the PSI. The data formats described below are encoded on a 5 MHz carrier using a self clocking bi-phase mark encoding scheme. The carrier is continuous. During idle periods, all "ones" are transmitted.

A frame consists of the following:

1	start bit	"0"
8	bit frame ID	
16	bit data field	twos compliment binary
8	bits unused	"0"
8	bit crc	error check ($x^8+x^7+x^5+x^4+x+1$ generating polynomial, excluding start and stop bits)
2	stop bits	ones
43	bits total	

It can also be viewed as shown in Figure 7.

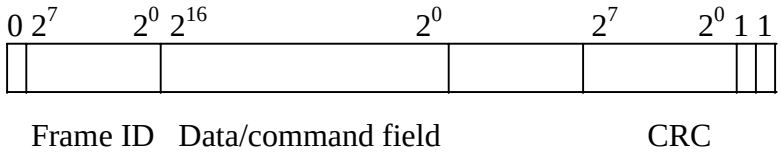


Figure 7. Typical Frame Layout

This frame layout is used for both transmissions from the PSC to the PSI and the reverse.

Data Sent from the PSC to the PSI

The data exchange between the PSC and the PSI starts with a single frame being transmitted from the PSC to the PSI. There are six possible frames, each with a unique frame ID. Each of these frames will cause one of three possible responses from the PSI.

The frames, with their IDs and PSI responses are listed in Table 1.

Table 1. Frames from the PSC to the PSI

Frame from PSC	ID (hex)	16 Bit Data Field	Response from PSI
Setpoint Without Read	55	two's complement binary	Echo Only
Setpoint With Read	15	two's complement binary	Status/ADC
Command Without Read	4A	see command definition	Echo Only
Command With Read	0A	see command definition	Status/ADC
Read Commands	00	not applicable	Command Reading
Read Status/ADC	40	not applicable	Status/ADC Reading

1. **Setpoint Without Read** - Data is sent to the D/A converter in the PSI. No information is returned except an echo of the sent Setpoint.

2. **Setpoint With Read** - Data is sent to the D/A converter in the PSI. An ADC conversion is initiated. Then, Status and the results of that conversion for all four ADCs are returned to the PSC.

3. **Command Without Read**- Data is sent to the Command bits of the PSI. No information is returned except an echo of the sent Command bits.

4. **Command With Read** - Data is sent to the Command bits of the PSI. An ADC conversion is initiated. Then, Status and the results of that conversion for all four ADCs are returned to the PSC.

5. **Read Commands** - This command sends no data to the PSI, but causes the Setpoint and Command registers on the PSI to be sent to the PSC.

6. **Read Status/ADC** - This command sends no data to the PSI, but causes an ADC conversion to be initiated. Then, Status and the results of that conversion for all four ADCs are returned to the PSC.

Data Sent from the PSI to the PSC

There are three possible responses from the PSI to the PSC.

1. **Echo Only -** Only the bits that were sent are echoed back to the PSC.

2. **Command Reading** - This message contains frames for an echo and the Setpoint and Command bits that are stored in the PSI.

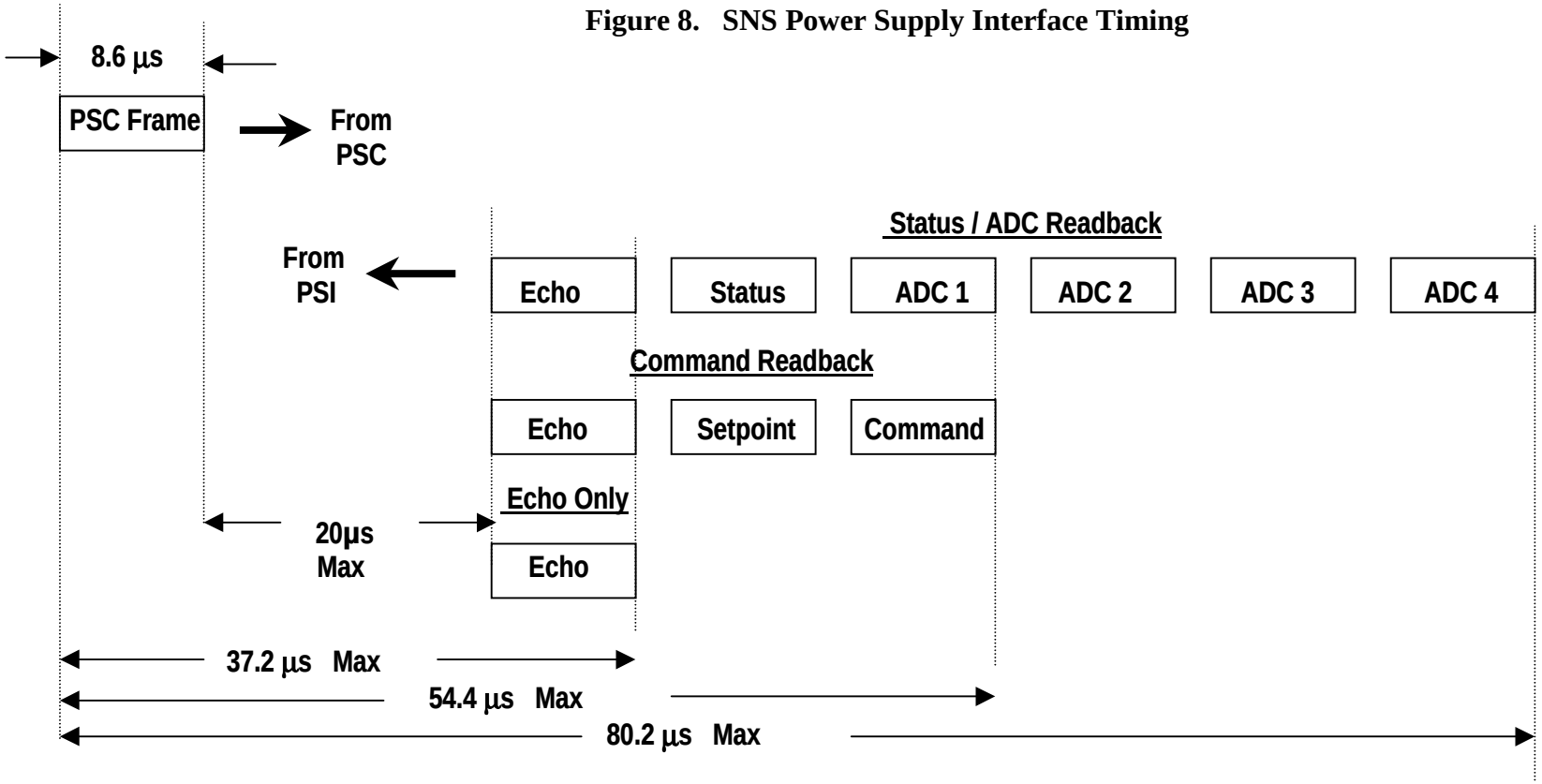
3. **Status/ADC Reading** - This message contains frames for an echo and the Status bits and the results of the ADC conversion for all four ADCs.

The details of these frames are shown in Table 2, and the timing is shown in Figure 8.

Table 2. Responses from the PSI

Response from PSI	Frame 1		Frame 2		Frame 3		Frame 4		Frame 5		Frame 6	
	ID (Hex)	Data	ID (Hex)	Data	ID (Hex)	Data	ID (Hex)	Data	ID (Hex)	Data	ID (Hex)	Data
Echo Only	ID Echo	Data Echo										
Command Reading	ID Echo	Data Echo	95	Command	8A	Setpoint						
Status/ADC Reading	ID Echo	Data Echo	93	Status	80	ADC A	90	ADC B	A0	ADC C	B0	ADC D

Figure 8. SNS Power Supply Interface Timing



Data Fields

Data Field for Command frame

2^{15} 2^{14}	2^{12}-2^{0}	Command
1 1	don't care	ON - Turns the power supply on.
0 0	don't care	OFF - Turns the power supply off.
0 1	don't care	STANDBY - Turns on control power in the supply, but does not energize the magnet load. In some supplies, this also resets faults.
1 0	don't care	RESET - Resets faults in supplies that require a separate line.
2^{13}		NEGATIVE - Indicates the power supply is in the reverse polarity

Data Field for Status frame

Bit	Command
2^{15}	ON - Indicates that the power supply is on and delivering power to the magnet load.
2^{14}	OFF - Indicates that control power to the power supply is off, but AC power is available.
2^{13}	STANDBY - Indicates that control power to the power supply is on, but no power is being sent to the magnet load.
2^{12}	NEGATIVE - Indicates the power supply is in the reverse polarity.
2^{11}	FAULT SUMMARY - Indicates that a fault has shut down the power supply regardless of which fault it was.
2^{10}	OVERVOLTAGE - Indicates that the power supply output voltage has exceeded it's set limit.
2^{9}	OVERCURRENT - Indicates that the power supply output current has exceeded it's set limit.
2^{8}	OUT OF REGULATION - Indicates that the current loop error is outside of acceptable limits.
2^{7}	FAN FAULT - Indicates loss of air flow.
2^{6}	OVERTEMP - Indicates excessive temperature anywhere in the power supply.
2^{5}	WATER FLOW - Indicates loss of water flow.
2^{4}	WATER MAT - Indicates water on the water mat, identifying a leak.
2^{3}	SECURITY INTERLOCK - Indicates the power supply was shut down as a result of opening an external interlock contact.
2^{2}	GROUND FAULT - Indicates a unwanted leakage path to ground.
2^{1}	RIPPLE FAULT - Indicates excessive ripple, identifying a misfiring or failed SCR in a phase controlled power supply.
2^{0}	PHASE FAULT - Indicates a lost phase or phase reversal.